In the Claims

Cancel claims 2 and 11, and amend claims 1 and 8-21 as follows:

1. (currently amended) A process for controlling focus parameters in a lithographic process used in manufacture of microelectronic circuits comprising:

providing a semiconductor wafer substrate on which there are to be lithographically formed functional circuit elements;

providing a lithographic mask having a target mask portion containing a measurable dimension sensitive to defocus;

projecting an energy beam through the target mask portion onto a first location of ~~a~~ the substrate at a first focus setting;

lithographically forming a first focus setting target on the substrate corresponding to the first focus setting, the first target containing a measurable dimension sensitive to defocus;

projecting an energy beam through the target mask portion onto a second location of the substrate at a second focus setting;

lithographically forming a second focus setting target on the substrate corresponding to the second focus setting, the second target containing a measurable dimension sensitive to defocus;

measuring the defocus sensitive dimension for each of the first and second targets on the substrate and comparing the defocus sensitive dimension of the first and second targets; and

determining a desired focus setting of the energy beam based on the comparison of the dimensions of the first and second focus setting target; and

using the determination of the desired focus setting of the energy beam to correct energy beam focus during lithographic forming of the functional circuit elements on the wafer substrate.

2. (cancelled)

3. (original) The process of claim 1 wherein the targets comprise a plurality of spaced elements having essentially the same length and width and forming an array, ends of the individual elements being aligned to form first and second opposing array edges, the array elements having a predefined pitch.

4. (original) The process of claim 3 wherein the defocus sensitive dimension measured and compared for each of the first and second targets on the substrate is the width of the array.

5. (original) The process of claim 1 wherein the targets comprise first and second complementary, tone reversed target portions, the first target portion comprising a plurality of spaced element shapes having essentially the same length and width and forming an array, the second target portion comprising a plurality of spaced element spaces having essentially the same length and width and forming an array, the first target portion element shapes being of contrasting tone to the second target portion element spaces, ends of the individual elements in each target portion being aligned to form first and second opposing array edges, the array elements having a predefined pitch.

6. (original) The process of claim 5 wherein the defocus sensitive dimension measured and compared for each of the first and second targets on the substrate is the width of the array.

7. (original) The process of claim 1 wherein the energy beam is projected through the target mask portion onto a plurality of substrate locations at a plurality of focus settings to create a plurality of targets, and wherein the widths of the individual targets are measured and compared to determine the desired focus of the energy beam.

8. (original) The process of claim 6 wherein the plurality of energy beam focus settings are distributed at predetermined positive and negative increments around an initial focus setting.

~~8~~9. (currently amended) The process of claim 1 ~~wherein the process is used to form a plurality of focus setting targets on a semiconductor wafer for use in manufacture of microelectronic circuits,~~ and wherein at least one of the focus setting targets is lithographically formed simultaneously with forming the functional lithographic circuit elements on the wafer substrate.

~~9~~10. (currently amended) The process of claim ~~8~~ 9 wherein the focus setting targets are formed at locations on the wafer substrate away from the functional lithographic circuit elements such that the functional lithographic circuit elements may be separated from the focus setting targets when the wafer is cut apart.

~~10~~11. (cancelled)

~~11~~12. (currently amended) The process of claim 1 wherein the target mask portion and the targets formed on the substrate each comprise a first area having a set of parallel array elements and a second, contrasting area having a set of contrasting parallel array elements parallel the array elements on the first contrasting area, and wherein target defocus sensitive dimension is measured by determining the distance between ends of the array elements on each of the first and second contrasting areas.

~~12~~13. (currently amended) The process of claim 1 wherein the determination of the desired focus setting of the energy beam is based both ~~the~~ on sign and magnitude of a focus correction feedback.

~~13~~14. (currently amended) The process of claim ~~12~~ 13 wherein the focus correction feedback is based on a negative offset target defocus and a positive offset target defocus.

~~14~~15. (currently amended) The process of claim ~~12~~ 13 wherein a dose correction is made simultaneously with the focus correction based on a measurement of the first and second targets on the substrate.

~~15~~16. (currently amended) A process for forming focus setting targets on a semiconductor wafer and controlling focus parameters in a lithographic process used in manufacture of functional microelectronic circuit elements comprising:

providing a semiconductor wafer substrate on which there are to be lithographically formed functional circuit elements;

providing a lithographic mask having a target mask comprising first and second target mask portions, the first target mask portion comprising a plurality of opaque, spaced element shapes having essentially the same length and width and forming an array, the second target mask portion comprising a plurality of transparent, spaced element spaces having essentially the same length and width and forming an array, ends of the individual elements in each target portion being aligned to form first and second opposing array edges, the array elements having a predefined pitch, the width between the array edges being sensitive to defocus when printed on a substrate;

projecting an energy beam through the target mask portion onto a first location of ~~a~~ the substrate at a first focus setting;

lithographically forming a first target on the substrate corresponding to the target mask at a first focus setting, the first target having complementary, tone reversed target array portions containing a measurable width between the target array edges sensitive to defocus;

projecting an energy beam through the target mask portion onto a second location of the substrate at a second focus setting;

lithographically forming a second target on the substrate corresponding to the target mask at a second focus setting, the second target having complementary,

tone reversed target array portions containing a measurable width between the target array edges sensitive to defocus;

measuring the width between the target array edges for each of the first and second targets on the substrate and comparing the target array edge width of the first and second targets;

determining a desired focus setting of the energy beam based on the comparison of the dimensions of the first and second target array widths; and

using the determination of the desired focus setting of the energy beam to correct energy beam focus during lithographic forming of the functional circuit elements.

~~16~~17. (currently amended) The process of claim ~~15~~ 16 wherein the energy beam is projected through the target mask portion onto a plurality of substrate locations at a plurality of focus settings to create a plurality of targets, and wherein the widths of the individual target arrays are measured and compared to determine the desired focus of the energy beam.

~~17~~18. (currently amended) The process of claim ~~16~~ 17 wherein the plurality of energy beam focus settings are distributed at predetermined positive and negative increments around an initial focus setting.

~~18~~19. (currently amended) The process of claim ~~15~~ 16 wherein the process is used to form a plurality of focus setting targets on a semiconductor wafer for use in manufacture of microelectronic circuits, and wherein at least one of the focus setting

targets is lithographically formed simultaneously with, and at locations on the wafer away from, functional lithographic circuit elements on the wafer such that the functional lithographic circuit elements may be separated from the focus setting targets when the wafer is cut apart.

~~19~~20. (currently amended) The process of claim ~~15~~ 16 wherein the determination of the desired focus setting of the energy beam is based both ~~the~~ on sign and magnitude of a focus correction feedback.

~~20~~21. (currently amended) The process of claim ~~19~~ 20 wherein the focus correction feedback is based on a negative offset target defocus and a positive offset target defocus.

~~21~~22. (currently amended) The process of claim ~~19~~ 20 wherein a dose correction is made simultaneously with the focus correction based on a measurement of the first and second targets on the substrate.